IN THE CLAIMS:

1. (Original) A system comprising:

an interrupt controller;

one or more interrupt request lines;

one or more multiplex blocks coupled with the interrupt controller and the one or more interrupt request lines, each of the one or more multiplex blocks corresponding to a distinct one of the one or more interrupt request lines; and

a virtual machine monitor (VMM) block coupled to the one or more multiplex blocks and a processor,

wherein each of the one or more multiplex blocks is to route an interrupt request signal received via a corresponding interrupt request line either to the interrupt controller or the VMM block depending on a current configuration value of said each of the one or more multiplex blocks.

2. (Original) The system of claim 1 wherein the current configuration value of said each of the one or more multiplex blocks requires that the interrupt request signal be routed to the interrupt controller if a device generating the interrupt request signal is managed by a currently operating virtual machine (VM).

3. (Original) The system of claim 1 wherein the current configuration value of said each of the one or more multiplex blocks requires that the interrupt request

signal be routed to the VMM block if a device generating the interrupt request signal is not managed by a currently operating virtual machine (VM).

4. (Original) The system of claim 1 wherein the VMM block comprises a mask register to store mask information pertaining to one or more interrupt request signals routed to the VMM block.

5. (Original) The system of claim 1 wherein the VMM block comprises a status register to store status of each interrupt request signal routed to the VMM block.

6. (Original) The system of claim 4 wherein the VMM block is to assert an internal signal if one of the one or more routed interrupt request signals is asserted and is not masked, and to send the internal signal to the processor to cause a transition of control to a VMM.

7. (Original) The system of claim 6 wherein the VMM block is further to combine the internal signal with an external signal generated by an external signal source prior to sending the internal signal to the processor.

8. (Original) The system of claim 7 wherein:

the external signal is a non-maskable interrupt (NMI) signal; and

the external signal source is a NMI source.

9. (Original) The system of claim 7 wherein the internal signal is combined with the external signal using an OR operator.

10. (Original) The system of claim 1 wherein the interrupt controller has a read and write access path to a plurality of registers of the interface controller.

11. (Original) The system of claim 1 wherein:

the one or more multiplex blocks are configurable by a virtual machine monitor (VMM).

12. (Original) The system of claim 4 wherein the mask register of the VMM block is configurable by a VMM.

13-18. (Cancelled)

19. (Original) An apparatus comprising:

one or more multiplex blocks coupled with an interrupt controller and one or more interrupt request lines, each of the one or more multiplex blocks corresponding to a distinct one of the one or more interrupt request lines; and

a virtual machine monitor (VMM) block coupled to the one or more multiplex blocks,

wherein each of the one or more multiplex blocks is to route an interrupt request signal received via a corresponding interrupt request line either to the interrupt controller or the VMM block depending on a current configuration value of said each of the one or more multiplex blocks.

20. (Original) The apparatus of claim 19 wherein the current configuration value of said each of the one or more multiplex blocks requires that the interrupt request signal be routed to the interrupt controller if a device generating the interrupt request signal is managed by a currently operating virtual machine (VM).

21. (Original) The apparatus of claim 19 wherein the current configuration value of said each of the one or more multiplex blocks requires that the interrupt request signal be routed to the VMM block if a device generating the interrupt request signal is not managed by a currently operating virtual machine (VM).

22-24. (Cancelled)

25. (Currently amended) A system comprising:

a processor; and

a memory, coupled to the processor, to store instructions, which when executed by the processor, cause the processor to identify one or more interrupt request lines that are coupled to one or more devices managed by a virtual machine

(VM), configure one or more multiplex blocks to route interrupt request signals that are managed by the VM on the one or more interrupt request lines to an interrupt controller, configure one or more multiplex blocks to route interrupt request signals that are not managed by the VM to a virtual machine monitor (VMM) block, and generate a request to transfer control to the VM.

26. (Currently amended) The system of claim 25 wherein the instructions, when executed by the processor, cause the processor further to ~~configure one or more multiplex blocks to route interrupt request signals that are not managed by the VM to a virtual machine monitor (VMM) block, and~~ configure a mask register in the VMM block to cause masking of interrupt request signals routed to the VMM block.

27. (Original) The system of claim 25 wherein the instructions, when executed by the processor, cause the processor further to restore a state saved during a previous operation of the VM in the interrupt controller.

28-30. (Cancelled)